In the Specification

Please replace the paragraph beginning on page 3, line 24 and ending on page 4, line 4 with the following amended paragraph.

In another embodiment, a computer system for generating a testbench is provided. The computer system includes a processor and memory. The memory includes mechanisms for holding information associated with the library of [[of]] modules. The processor is configured to generate a plurality of test designs. The plurality of test designs have varied characteristics to allow substantial testing of a design automation tool. Generating one of the plurality of test designs includes instantiating the I/O structure of a top level module, parameterizing submodules from a design module library, and providing logic to interconnect the plurality of parameterized submodules. The top level module has input and output pins. The plurality of submodules from a design module library are parameterized for interconnection with the top level module. The plurality of submodules have input and output lines. Logic is provided to interconnect the plurality of parameterized submodules as well as to connect the plurality of parameterized submodules to various input and output pins of the top level module.

Please replace the paragraph beginning on page 15, line 9 and ending on page 15, line 24 with the following amended paragraph.

Figure 6 is a process flow diagram showing one exemplary technique for selecting submodules. At 603, a library of submodules is identified. According to various embodiments, a library of submodules corresponds to a particular device ~~classes are~~ class or device family. At 605, the type, cost, and maximum instantiation limitations are identified for the various modules. In many examples, the type, cost, and maximum instantiation information is included in a module registry 663. At 607, a probabilistic function is applied to select modules of different types from the library of submodules. For example, the user may specify that various memory modules have a 25 percent chance of being selected. A particular phase locked loop module may have a six percent chance of being selected. A probabilistic function is used to select particular submodules from the module library. At 609, cost constraints are applied as needed to reduce the set of

selected modules. For example, if a device class supports only two kilobytes memory, no more than two kilobytes worth of memory modules will be selected. At 611, maximum instantiation constraints are applied to further reduce the set of selected modules. For example, a particular device may be limited to two DSP cores.